Amendments to the Claims:

Claim 1 (original) An apparatus for verification of redundant functions on a circuit, comprising:

a circuit function block having nodes, the nodes arranged to access each of the redundant functions on the circuit;

a test interface circuit including an input and an output, the input arranged to receive an input signal, and in response to the input signal, supply a test signal, indicating a function on the circuit to test, and

the circuit function block arranged to receive the test signal, and in response to the test signal couple at least one of the nodes within the circuit function block to the output test interface such that the function may be tested.

Claim 2 (original) The apparatus of Claim 1, wherein the circuit function block, further comprises:

a functional block, arranged to receive the test signal, and in response to the test signal couple at least one node within the functional block to the output of the test interface such that the function may be tested; and

a redundant functional block, arranged to receive the test signal, and in response to the test signal couple at least one corresponding node to the output of the test interface such that the function may be tested, the at least one corresponding node accessing the same relative location within the redundant functional block as the at least one node within the functional block.

Claim 3 (original) The apparatus of Claim 2, further comprising, a controller circuit arranged to receive the test signal and in response to the control signal selectively couple the at least one of the nodes within the functional block and the at least one of the corresponding nodes within the redundant functional block to the output of the test interface.

Claim 4 (original) The apparatus of Claim 3, wherein the test interface comprises a plurality of input pins and a plurality of output pins, each of the input pins arranged to receive the test signal, and each of the output pins arranged to provide an external signal.

Claim 5 (original) The apparatus of Claim 4, wherein the test interface further comprises:

an input test interface arranged to receive the input signal and output the test signal; and

an output test interface arranged to output the external signal.

Claim 6 (original) An apparatus for redundant function verification for an integrated circuit, the circuit a mixed signal circuit and configuration, control and testing circuitry for the mixed signal circuit, comprising:

a protocol logic interface circuit arranged to receive a control signal and arranged to activate a test mode within the circuit in response to the control signal, the test mode arranged to test a functional block and a redundant functional block within the circuit;

a mixed signal circuit including access lines to internal nodes and external nodes of the integrated circuit; the internal nodes and the external nodes selected in response to the test mode;

a switch circuit coupled between output pins and the internal and external nodes, respectively, the switch circuit arranged to connect the internal nodes and external nodes to the output pins in response to the test mode to test the functional block and the redundant functional block within the circuit.

Claim 7 (original) The apparatus of Claim 6, further comprising, a memory circuit arranged to store configuration information in response to the test mode.

Claim 8 (original) The apparatus of Claim 7, wherein the protocol logic interface circuit, further comprises:

a lock enable circuit arranged to receive a lock enable signal;

a lock circuit coupled to the lock enable circuit and arranged to receive the lock enable signal and produce a valid key signal in response to the lock enable signal.

Claim 9 (original) The apparatus of Claim 8, further comprising a decoder circuit, the decoder circuit coupled to the lock circuit and arranged to receive the valid key signal and the control signal, the decoder circuit arranged to configure the test mode in response to the valid key signal and the control signal.

Claim 10 (Currently Amended) A method for verifying redundancy of a functional block within a circuit, comprising:

receiving an input signal at a test interface circuit and from the test interface circuit supplying a test signal indicating a function on the circuit to test;

receiving the test signal at a circuit function block, wherein the circuit function block includes nodes arranged to access each of the redundant functions on the circuit;

in response to the test signal, coupling at least one of the nodes within the circuit function block to an output of the test interface circuit such that the function may be tested;

~~(a) creating a test to verify the redundancy of the functional block within the circuit;~~

~~(b) performing the test~~ testing the function to verify the redundancy of the functional block within the circuit; and

~~(c)~~ determining if the functional block circuit passed the test.

Claim 11 (original) The method of Claim 10, further comprising, when the functional block passed the test approving the circuit, otherwise, rejecting the circuit.

Claim 12 (original) The method of Claim 11, wherein performing the test to verify the redundancy of the functional block within the circuit, comprises performing the test on each of the corresponding functional blocks that are redundant within the circuit.

Claim 13 (original) The method of Claim 12, wherein performing the test to verify the redundancy of the functional block within the circuit, further comprises:

coupling at least one test mode pin to a node within the circuit based on the test; and

performing the test through the use the at least one test mode pin.

Claim 14 (original) An apparatus to verify the redundancy of functions included on an integrated circuit with a mixed signal circuit and configuration, a control and testing circuit for the mixed signal circuit, comprising:

input terminals arranged to convey input signals and configuration control signals;

interface terminals arranged to convey the interface signals and analog interface signals;

an interface circuit coupled to the input terminals that is arranged to provide configuration data and switch control signals in response to the configuration control signals, the configuration; and

an analog circuit with redundant functions, the analog circuit including internal nodes and external circuit terminals within each of the redundant functions, coupled to the interface circuit, that is arranged to communicate internal analog signals and external analog signals via the internals nodes and external circuit terminals to each of the redundant functions, in response to a portion of the configuration data.

Claim 15 (original) The apparatus of Claim 14, further comprising:

a switching circuit that is arranged to alternately couple respective ones of the internal and the external circuit terminals in response to the switch control signals;

wherein respective ones of the internal analog signals and the external analog signals change in response to corresponding changes in respective ones of the portion of the configuration data.

Claim 16 (original) The apparatus of Claim 15, further comprising a memory circuit, coupled to the interface circuitry and the analog circuit, that stores the configuration data.

Claim 17 (original) The apparatus of Claim 14, wherein the interface circuitry comprises a data decoding circuit that is coupled to the input terminals and decodes the configuration control signals and is arranged to provide the configuration data and the switch control signals.

Claim 18 (original) The apparatus of Claim 17, wherein the interface circuitry further comprises, a lock decoding circuit that is coupled between the input terminals and the data decoding circuit that is arranged to enable and disable the data decoding circuit in response to the configuration control signals.

Claim 19 (original) The apparatus of Claim 18, wherein the switching circuit comprises a plurality of switch circuits.

Claim 20 (original) The apparatus of Claim 17, further comprising, a mode control circuit, coupled to the interface circuit and provides the test mode control signals in response to the enablement of the data decoding circuit.

Claim 21 (Currently Amended) An apparatus for verifying redundancy of a function on a circuit, comprising:

a means for receiving an input signal at a test interface circuit and supplying a test signal indicating a function on the circuit to test;

a means for receiving the test signal at a circuit function block, wherein the circuit function block includes nodes arranged to access each of the redundant functions on the circuit;

in response to the test signal, a means for coupling at least one of the nodes within the circuit function block to an output of the test interface circuit such that the function may be tested;

~~a means for accessing a plurality of occurrences of the function on the circuit;~~

a means for performing at least one test to verify the redundancy of the function on the circuit; and

a means for determining if the plurality of the occurrences of the function on the circuit passed the at least one test.

Claim 22 (original) The apparatus of Claim 21, further comprising, when the plurality of the occurrences of the function on the circuit passed the at least one test, a means for approving the circuit, otherwise, a means for rejecting the circuit.